Jul 2007

Q-Switch Driver

Including: AOQ Alignment

Instruction Manual

AQS1100D

Models -

AQSR1100D-27 : Dual 110W output , 27MHz

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Blackwood EMC

Certificate of Test

Certificate No: C 06-0563A
This Certificate is dated: 13 October 2006

Issued to:	Isomet (UK) Ltd 18 John Baker Close Llantarnam Park Cwmbran NP44 3AX
Job Number:	06-0563A
Equipment Tested:	Dual Output Q-Switch Driver
Model Number:	AQS1100D
Sample reference(s):	862690
Date(s) of test:	12th & 13th September 2006

This is to certify that the equipment defined above was tested by Blackwood EMC Ltd at the EMC laboratory at Unit 8 Woodfieldside Business Park, Pontllanfraith, Blackwood, NP12 2DG, UK, in accordance with the following specifications:

Electromagnetic Compatibility:

EN 55022:1998 + A1:2000 + A2:2003
EN 55024:1998 + A1:2001 + A2:2003
EN61000-3-2:2000
EN61000-3-3:1995 +A1:2001

The sample(s) tested were compliant to the above specifications(s).
The result relates only to the item(s) tested
Full details are given in Blackwood EMC Test Report R 06-0563A

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Technical Manager, Blackwood EMC Ltd

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1. GENERAL

The AQS1100D dual output RF driver features a common waveform generator, RF oscillator, and DC power supply in an industry standard 3U 19" rack.

This driver features Isomet's "Soft-Start" RF amplitude control. The Soft-Start technique applies a mix of digital and analog modulation signals to control the RF amplitude. Almost any envelope or ramp shape can be programmed.

Output timing and pulse widths can be controlled either by an internal PLL based waveform generator or from a user supplied external signal(s) source.

The driver incorporates opto-isolated digital I/O signals and output protection.
This includes:

- load mismatch / poor VSWR detection *
- driver over-temperature interlock
- temperature compensation
- two external interlocks (e.g. for connection to the AO device thermal switch)

In addition each PA section provides analog voltages proportional to the forward and reverse power plus a thermistor resistance proportional to temperature.

The AQS1100D will operate from a 110-260Vac, 50/60Hz, 3A supply

Output status bits are supplemented by LED's. These indicate the operating condition of the driver and associated Q-switches.

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1.1 MODEL SELECTION

		Freq		Option	Q-Switch
AQSR1100D	-	FC	-	x	Isomet Q1083 series
24.0MHz		24			
27.12MHz		27			

2. DESCRIPTION

Figure 1 (page 17) shows the driver rack.

A driver schematic is given in Figure 2. The RF centre frequency is derived from a common crystal controlled oscillator(s). The digital modulation signal and the analog slope signal are combined in a high speed op-amp A1. This op amp controls the RF amplitude via a double balanced mixer.

The maximum output power for each RF output can be adjusted by one of two methods:

a, Pre-set potentiometers, one for each output accessible on the front panel

b, Digital potentiometers, one per output. This allows remote power adjustment via J5. The user can select which method is active.

Figure 3 shows the connection table and typical alignment set-up

Figure 4 describes the fundamental equations for AOQ switch operating in the Bragg regime.

There are a variety of operating modes available with AQS1100D range of driver racks.

Signals to control the modulation parameters of the RF can be internally generated or applied from an external source.

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2.1 Connector Summary

Details below give the basic configuration for the driver rack, preliminary connector positions and pin assignments. See Figure 1

Key:

Type

I	:	Isolated
N	:	Non-isolated
D	:	Digital
P	:	Power
A	:	Analogue
R	:	Reference
I	:	n to isomet
o	:	out from Isomet

Connectors J1 , J2

BNC 50ohm
RF outputs

Connectors J3 , J4

9way female D-type
Power Amp Monitoring PA1 (PA2)

Signal	Type	Pin
24V / 80mA dc out	NPo	1
0Vdc	NP	6
Reverse Power 1 (2)	NAo	2
0V	NP	7
Forward Power 1 (2)	NAo	3
0V	NR	8
5Kohm NTC Thermistor + 1 (2)	IAo	4
		9
Thermistor - 1 (2)	IAo	5

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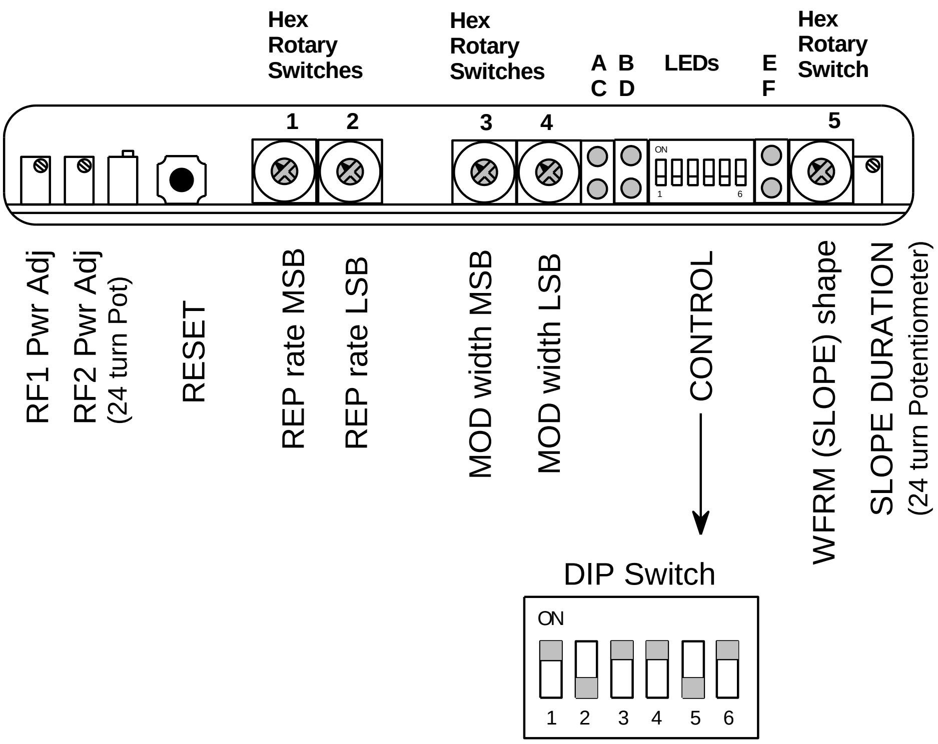
Connector J5

37way **female** D-type
Driver control

Signal	Active	Note	Type	Pin
-DigPot_PA1_WE	L/H	H = Mem, L = Adj	IDi	1
0V			IR	20
-Inc Clock	↓	Incremental Clock, R/100 steps	IDi	2
0V			IR	21
Up/-Down	H/L	Pot adjustment direction	IDi	3
0V			IR	22
-DigPot_En	LOW	Low = O/P power set by Digital Pots	IDi	4
0V			IR	23
-DigPot_PA2_WE	L/H	H = Mem, L = Adj	IDi	5
0V			IR	24
-SB4	X	Composite pulse/FPC sync.	IDo	6
0V			IR	25
-SB3	LOW	(-Err3)	IDo	7
0V			IR	26
-Reset	LOW	Reset	IDi	8
0V			IR	27
Slope_Mod_En	LOW	*Enable ramped modulation depth*	*IDi*	9
0V			IR	28
-SB2	LOW	(-Err2)	IDo	10
0V			IR	29
-SB1	LOW	(-Err1)	IDo	11
0V			IR	30
PSU Status	HIGH	Unit Power On	IDo	12
0V			IR	31
nc		*Nc*	IDi	13
0V			IR	32
AOQ1_OT	LOW	Normally closed = OK	IDi	14
0V			IR	33
AOQ2_OT	LOW	Normally closed = OK	IDi	15
V			IR	34
START	↑	(FPC Trigger)	IDi	16
0V			IR	35
Ext Rep Rate	↑	(Pulse Trigger)	IDi	17
0V			IR	36
-RF Enable1	LOW	Enable PA1	IDi	18
0V			IR	37
-RF Enable2	LOW	Enable PA2	IDi	19

3.0 Controls



3.1 DIP switch functions

	UP	DOWN
SW1	***RF On J1***	RF Off J1
SW2	CW RF	***Modulated RF***
SW3	**External PRF**	Internal PRF
SW4	**Rep_rate / 10**	*Base Rep_rate*
SW5	SLOPE Duration x10	***Base Timing***
SW6	***RF On J2***	RF Off J2

Default settings in ***Bold***

SW1 DOWN will turn the RF output J1 OFF, regardless of other settings.

SW2 UP will force the driver to output a constant (CW) RF power regardless of the modulation inputs. This can be used to force the AOQ on and thus the laser output to zero.

SW3 selects the modulation trigger source. If Internal, PRF is set by Hex_SW1 and SW2.

SW4 divide the rep-rate frequency (See section 3.3)

SW5 UP increases the SLOPE duration by 10x (See section 3.2)

SW6 DOWN will turn the RF output J1 OFF, regardless of other settings.

Note: A Low Forward Power or High Reflected Power fault condition can be cleared by toggling either SW1 or SW6

3.2 WFRM SLOPE Specifications

Hex SW 5 Position	Slope shape	Duration Multi-Turn Pot adjustment range (DIP-SW 5 ***Down***)
0	Pseudo Linear 90% Truncated	75usec – 343usec
1	Mod-Linear	75usec – 343usec
2	Pseudo Linear 80% Truncated	75usec – 343usec
3	*Offset Exponential*	*75usec – 343usec*
4	Exponential	75usec – 343usec
5	Cosine	75usec – 343usec
6	Pseudo Linear 70% Truncated	75usec – 343usec
7	Pseudo Linear 60% Truncated	75usec – 343usec
8	Pseudo Linear	75usec – 343usec
9	Pseudo Linear 50% Truncated	75usec – 343usec
A	Pseudo Linear 40% Truncated	75usec – 343usec
B	Sine-Linear	75usec – 343usec
C	Pseudo Linear 30% Truncated	75usec – 343usec
D	Pseudo Linear 20% Truncated	75usec – 343usec
E	Pseudo Linear 10% Truncated	75usec – 343usec
F	None	(No START input required)

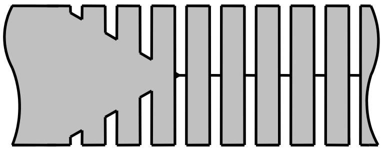
Durations are x10 longer with the Control DIP-SW 5 ***UP***

Shapes can be reprogrammed to suit customer requirements

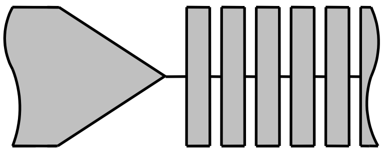
During the "Soft Start" slope, RF modulation can be enabled using the SLOPE MOD input pin-9 on the 37way D-type.

Options :

SLOPE MOD
Enabled
(pin 9 to pin 37)



SLOPE MOD
Disabled
(pin9 Open)



3.3 SETTING THE INTERNAL REP-RATE CONTROL

This is based a PLL controlled oscillator. The internal rep-rate set by HEX-SW 1 and 2

Output rate is further scaled by DIP-SW 4

SW 4 **UP**	:	Rep-rate increments in 0.05KHz steps
SW 4 **DOWN**	:	Rep-rate increments in 0.25KHz steps

Examples:

DIP Switch	Hex Switch	Rep- Rate	
Range setting	SW1 / SW2	KHz	
SW4 Up	F 2	1.5	Minimum stable rate for this range
	C 4	3.0	
	A 6	4.5	
	8 8	6.0	
	6 A	7.5	
	4 C	9.0	
	1 0	12.0	
SW4 DOWN	D 0	12.0	Minimum stable rate for this range
	C 8	14.0	
	C 0	16.0	
	B 8	18.0	
	B 0	20.0	
	8 8	30.0	
	6 0	40.0	
	3 8	50.0	
	1 0	60.0	Maximum stable rate

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3.4 SETTING THE INTERNAL PULSE WIDTH CONTROL

Based on a precision digital counter. Resolution = 61nsec steps.

Pulse width set by Hex_SW 3 and 4. Minimum pulse width = 1usec.

The RF OFF pulse width can be calculated from:

Pulse Width (us) = (255-N)*0.061 + 1

where N is the decimal value of Hex SW_3 (MSB) and SW_4 .

Examples:

	Hex Switch SW3 / SW4	N (Dec)	Pulse Width usec
(Minimum width)	F F	255	1.0
	E E	238	2.0
	C E	206	4.0
	6 B	107	10.0
(Max width)	0 0	0	16.6

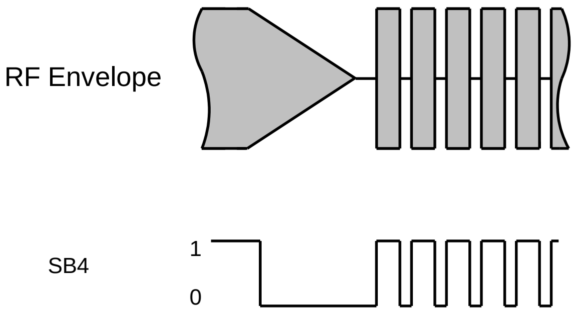
4.0 FAULT INDICATION, STATUS BITS AND LED'S

Viewing timing and pulse width of modulation signals.

A composite TTL waveform combining the SLOPE DURATION and the MODULATION pulse train is available on status bit SB4.

This can be used to view the modulation timing of the RF signal.

This signal is not generated when the External DIG MOD operating mode is selected.



4.1 Fault Status Bits

Status bits are available on the 37way D-type connector and supplemented using LED visible indicators. All signals are opto-isolated TTL . **Faults signals are prioritized**

Fault	LED					Status Bit			
	A	**B**	**D**	**C***		SB1 Pin11	SB2 Pin10	SB3 Pin7	SB4 Pin6
No Fault				G		H	H	H	-
Low Forward Power 1 (Lowest Priority)		R		G		L	H	H	-
Low Forward Power 2	R			G		H	L	H	-
Amplifier Temp Interlock	R	R		G		L	L	H	-
AOQ1 Temp Interlock			R	G		H	H	L	-
AOQ2 Temp Interlock		R	R	G		L	H	L	-
High Reverse Power 1 (Highest Priority)	R		R	G		H	L	L	-
High Reverse Power 2	R	R	R	G		L	L	L	-

LED code : R = Red illuminated , G = Green illuminated, Y = Yellow illuminated

* LED C : Green whilst RF is modulated low
Brightness will depend on the duty cycle of the RF output.

In addition to the Fault signals, two further LEDS indicate operation of the driver

LED E : Yellow ON when START input is low.
Brightness will depend on the duty cycle of the START input.

LED F : Yellow ON = RF Enabled.
Brightness will depend on whether one or both RF power amps are enabled.

5.0 Interlocks

BOTH thermal interlock inputs on the 37way D-type need to be connected to the AOQ thermal switches or connected to 0V at the 37way D-type connector.

Over temperature is a non latching condition. The driver will self reset if the thermal interlock cools to valid state following an over-temperature fault. i.e. switch from non-valid (open contact, over temperature state) to a valid (normally closed contact) condition.

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6.0 VSWR Indication

- Low Forward power

The Driver will generate a ***Low Forward Power*** fault signal if the transmitted RF output power falls below approximately 80W average RF power.
There is no effect on the driver operation.

- High reverse power.

The Driver will output a ***High Reverse Power*** fault signal if the average reflected RF power from the AOQ exceeds approximately 10% of the maximum CW driver RF forward power.
This fault is latching and the driver is disabled (RF power will be at zero).
This fault will also occur if the RF connection between the AOQ and driver is broken.

NOTE:
These faults are not effective if either amplifier is intentionally disabled using the -RF enable signals via the front panel DIP SW1 /SW6 or the respective signals on pins 18/19 of the 37way D-type.

Resetting

Once a fault condition is corrected, it will be necessary to reset the driver.

1: Turn the DC power OFF and ON or
2: Press RESET button on driver or
3: Momentarily make contact between pin 13 to pin 32 on the 37way D-type.

OR

4: Clear faults and re-enable output by toggling any -RF enable signal.
Thus,
- Toggle either SW1 or SW6
or
- Toggle levels on pin 18 or pin 19 of 37way D-type

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7. INSTALLATION AND ADJUSTMENT

The required RF modulation Pulse Width, WFRM shape and SLOPE duration are a function of the laser cavity gain and operating parameters. The procedure below outlines one technique for aligning the AOQ and setting the optimum RF drive power.

7.1 If applicable connect cooling water to the Q-switch at a flow not less than 0.5 litres/minute at < 27 deg.C.

Due to the high RF power dissipated in the water cooled AOQ switches, it is paramount that the AOQ is operated only when water cooling is circulating.

7.2 With no a-c power applied, connect the AC supply to the IEC socket on the real panel. DO NOT APPLY POWER.

7.3 Connect the BNC RF outputs to the acousto-optic Q-switches (or a 50Ω RF loads, if it is desired to measure the RF1 or RF2 output power).

7.4 If applicable connect the Interlock of the acousto-optic Q-switches to the enable inputs on the 37-pin D-type connector of the AQS driver.
If the temperature of the modulator exceeds 32ºC or the internal driver temperature exceeds 70ºC then the interlock connection becomes open circuit, disabling the RF output. An LED indicator illuminates when the Interlocks are closed and the RF is enabled. (see 4.1).

If there is no Interlock on the AO Q-switch, connect the AQS interlock inputs to 0V.

7.5 Adjustment of the RF output power is best done with amplifier connected to the acousto-optic Q-switch. The Amplifier maximum output power is factory preset to approx 2/3rds maximum output.

The optimum RF power level required for sufficient hold-off and stable Q-switch operation will depend on the laser cavity design and gain parameters. Applying RF power in excess of this optimum level may cause undesired thermal loading and possible unstable laser behaviour. It is therefore recommended that initial alignment be performed at a low RF power level.

7.6 Locate the PWR ADJ adjusters on the driver .
With an insulated alignment tool or screwdriver rotate the PWR ADJ1 and PWR ADJ2 potentiometers fully anti-clockwise (CCW) i.e. OFF, then clockwise (CW) approx 12 – 16 turns.

7.7 Apply AC power to the rack.

7.8 Apply a constant RF power to the AOQ by placing SW2 of the DIP switch in the UP position.

7.9 Align the laser beam toward the centre of (either) aperture of the AOQ. Refer to AOQ data sheet. Ensure the polarization is correct for the AOQ being used. Adjust the beam height so that it is central to the active aperture height of the AOQ.

7.10 Start with the laser beam normal to the input optical face of the AOM and very slowly rotate the AOM (either direction). See Figure 4 for one possible configuration.

Observe the CW laser output (= the undeflected zeroth order beam form the AOQ). Adjust the AOQ Bragg angle (rotate the device) to minimize the laser output beam intensity.
If no extinction is observed check the RF driver is operating and applying a CW RF signal to the AOQ. If this is OK, increase the RF power a little and repeat the procedure.

After the AOQ angle has been optimized, slowly increase the RF power by turning PWR ADJ clockwise until maximum extinction of the laser output is obtained.

On the threshold of the optimum RF power, the laser output will flicker On and Off

If possible adjust the beam height relative to the mounting surface in order to optimize efficiency.
The goal it to achieve the best hold off and extinction for the least RF drive power.

7.11 Introducing an AOQ into the laser cavity may affect the oscillation properties of the laser. This is due to the refractive index of the AOQ and consequential path length change. It is quite possible that a negative insertion loss is recorded simply by placing the AOQ into the laser cavity !

7.12 After the AOQ is introduced into the cavity, some adjustment of the laser mirror(s) may be required to peak the CW laser power, prior to AOQ operation.

8. MAINTENANCE

8.1 Cleaning

It is of utmost importance that the optical apertures of the AOQ are kept clean and free of contamination. When the device is not in use, the apertures may be protected by a covering of masking tape. When in use, frequently clean the apertures with a pressurized jet of filtered, dry air.

It will probably be necessary in time to wipe the coated window surfaces of atmospherically deposited films. Although the coatings are hard and durable, care must be taken to avoid gouging of the surface and leaving residues. It is suggested that the coatings be wiped with a soft ball of brushed (short fibres removed) cotton, slightly moistened with clean alcohol. Before the alcohol has had time to dry on the surface, wipe again with dry cotton in a smooth, continuous stroke. Examine the surface for residue and, if necessary, repeat the cleaning.

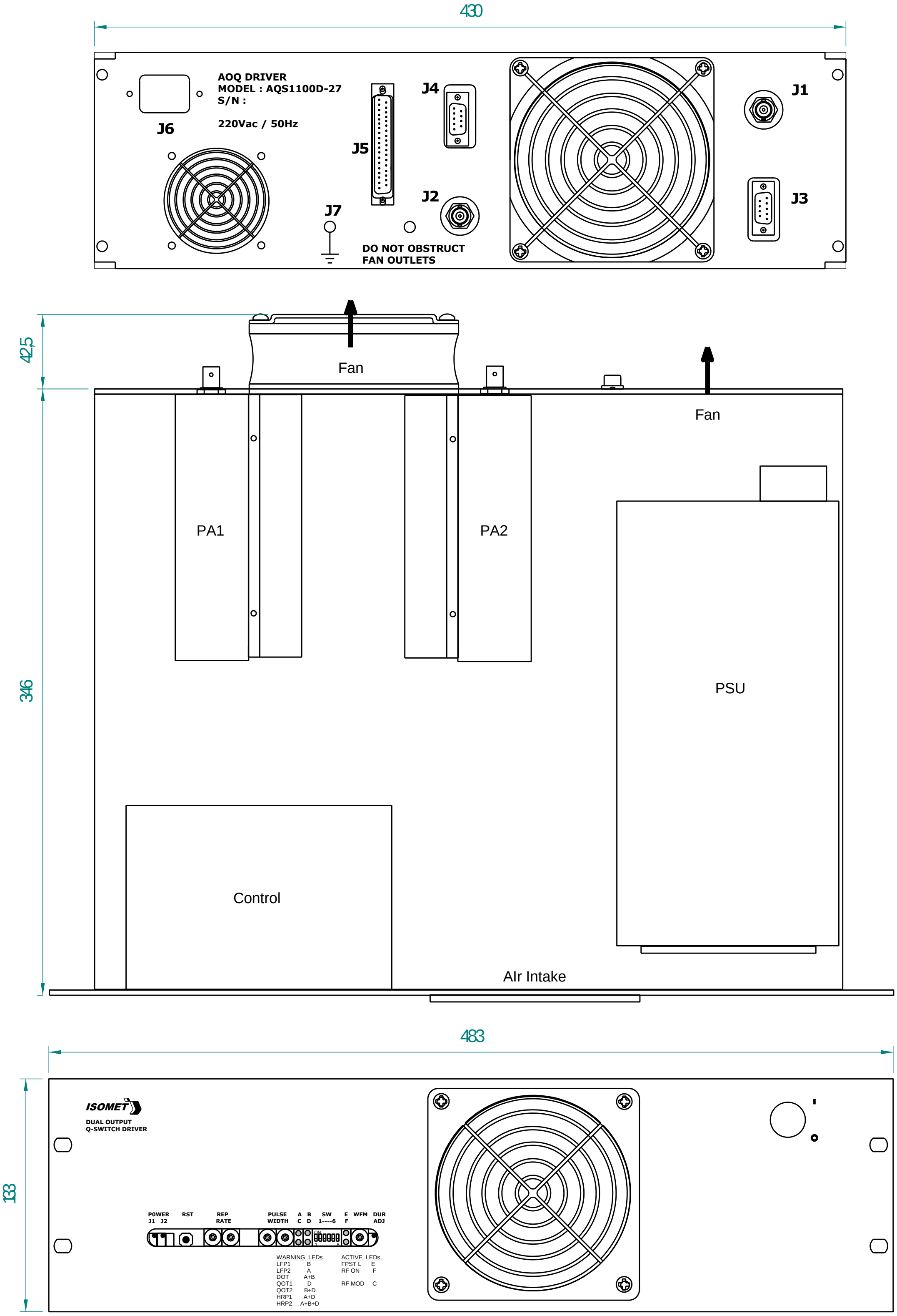
8.2 Troubleshooting

No troubleshooting procedures are proposed other than a check of alignment and operating procedure. If difficulties arise, take note of the symptoms and contact the manufacturer.

8.3 Repairs

In the event of deflector malfunction, discontinue operation and immediately contact the manufacturer or his representative. Due to the high sensitive of tuning procedures and the possible damage which may result, no user repairs are allowed. Evidence that an attempt has been made to open the optical head will void the manufacturer's warranty.

Figure 1: 19” Rack Outline



Dim’n : mm

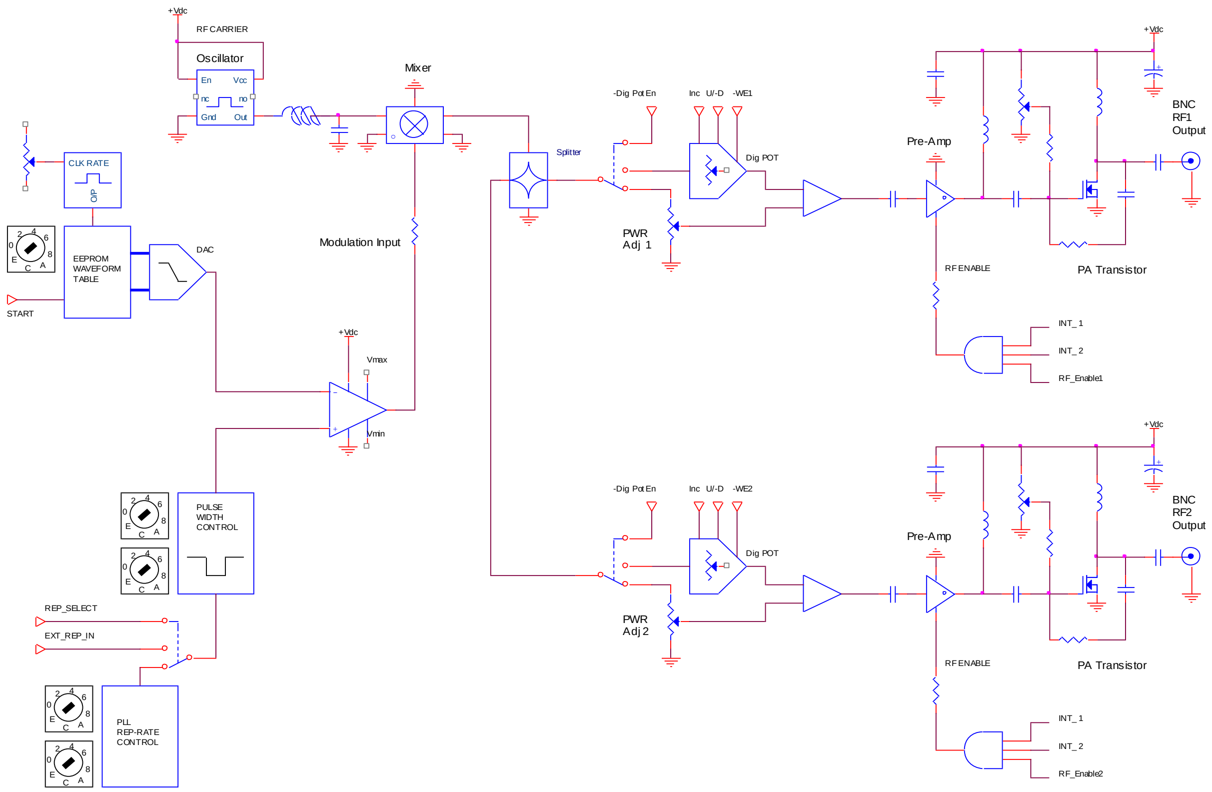
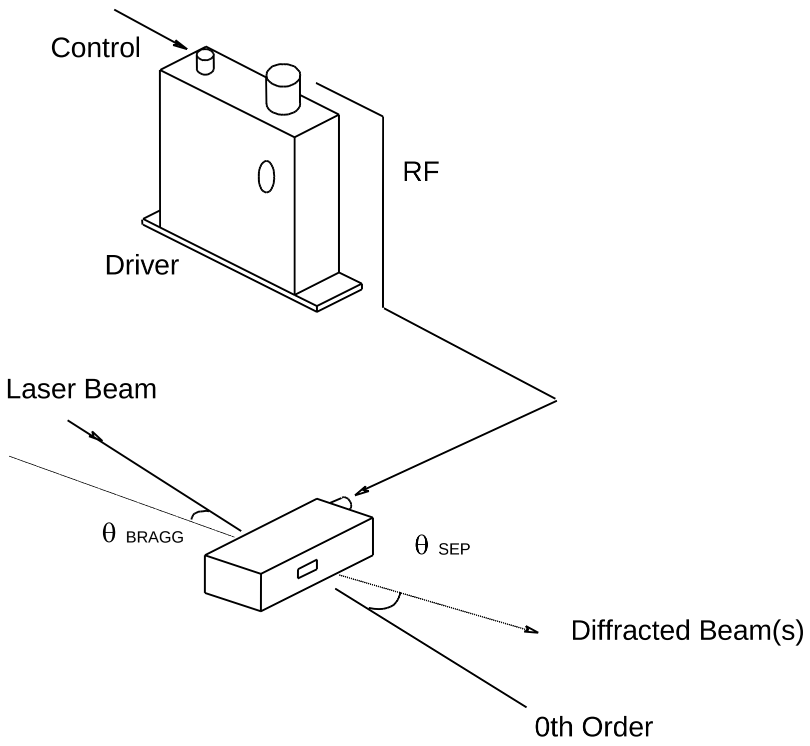


Figure 2: Driver Block Diagram.

Function	**Adjustment**	**Specification**
Rep Rate	8-bit via 2 Hex Rotary Switches 1 & 2 plus Range Select Switch	1 – 120KHz
Pulse Width	8-bit via 2 Hex Rotary Switches 3 & 4	1 – 16.5 usec
RF1 On/Off RF CW/Modulated Rep-Range Select (2) Slope-Range Select RF2 On/Off	DIL 6-way Lever Switch	Select Function
Waveform Shape	1 of 16 via Hex Rotary Switch 5	EPROM stored
Shape Period	24 turn potentiometer plus Range Select Switch	18usec – 13.7msec
RF Power	24 turn potentiometer	< 25% - 100%

Basic AO Q-Switch Parameters, operating in the Bragg Condition



The input Bragg angle, relative to a normal to the optical surface and in the plane of deflection is:

$$\theta_{BRAGG} = \frac{\lambda . fc}{2.v}$$

The separation angle between the Zeroth order and the +/- First orders is:

$$\theta_{SEP} = \frac{\lambda . fc}{v}$$

Optical rise time for a Gaussian input beam is approximately:

$$t_r = \frac{0.65.d}{v}$$

where: λ = wavelength
fc = centre frequency of AOQ = 24.0, 27.12, 40.68, or 80MHz
v = acoustic velocity of interaction material
= 4.2mm/usec (TeO2)
= 5.7mm/usec (a-Quartz)
= 5.96mm/usec (Fused Silica, Compressional mode)
= 3.76mm/usec (Fused Silica, Shear mode)

d = $1/e^2$ beam diameter

Figure 4. AOQ Equations