Mar 15

# Acousto-Optic Modulator Driver

**Including: Modulator Alignment**
**AOM750-H, M1192-G50, M1199-G50, M1315-G50**

# Instruction Manual

## RFA651 Series
## Analog Modulation, 50MHz Amplifier
## Remote I2C Power Level Control

Models -

RFA651-xxx : 50MHz, 180W output, 0-10V modulation

Options **–xxx**, combinations possible.

- D : TTL digital (On-Off) modulation
- DA : dual analog and TTL digital modulation
- BR : Brass water cooled heatsink (water fittings on rear face only)

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## 1. GENERAL

Key Features:

- 24Vdc, water cooled high power amplifier
- RF output >180W at 50.00MHz
- RF rise/fall time < 300/100nsec at 150W
- High Speed amplitude modulation
  RFA651: analog
  RFA651D: TTL digital
  RFA651DA: analog & TTL digital
- Modulation peak level is defined by two methods
  - Digitally programmed potentiometer stack
  - Manual adjustment potentiometer.
- Digital potentiometers programmed via buffered I2C interface
- Opto-isolated PLC compatible inputs on POT select and RF enable inputs.
  (Response time circa 1msec)
- Tri colour LED status indicator
- High VSWR shut-down protection

A block diagram of the driver is shown in Figure 3. The center frequencies are determined by free-running quartz-crystal oscillator. The frequency is accurate and stable to within ± 25ppm.
A high-frequency, diode ring modulator provides high speed amplitude modulation of the RF carrier. The peak RF power level for each frequency is set by a multi-turn manual potentiometer or by digitally controlled potentiometers.

## 2, CONTROL

Two inputs directly control the RF output; *Gate* and *Modulation*.

The relationship between the driver control inputs, the RF waveform and AO response is shown below for RFA651 driver with analog modulation.

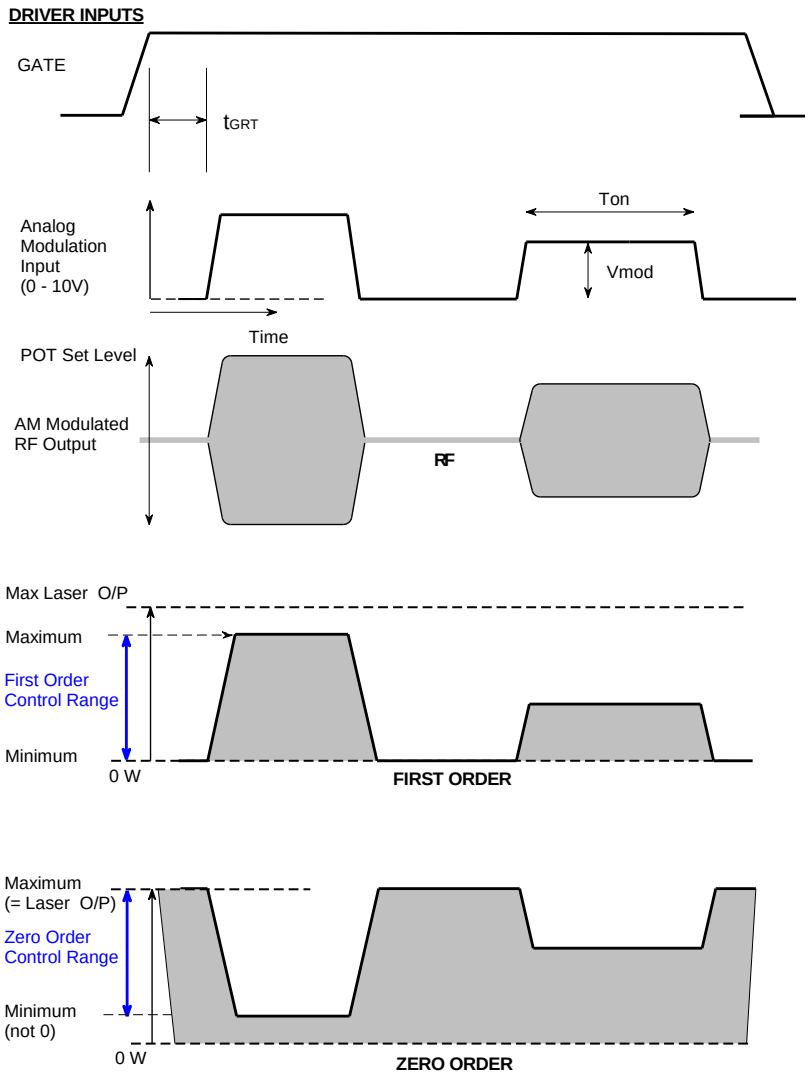
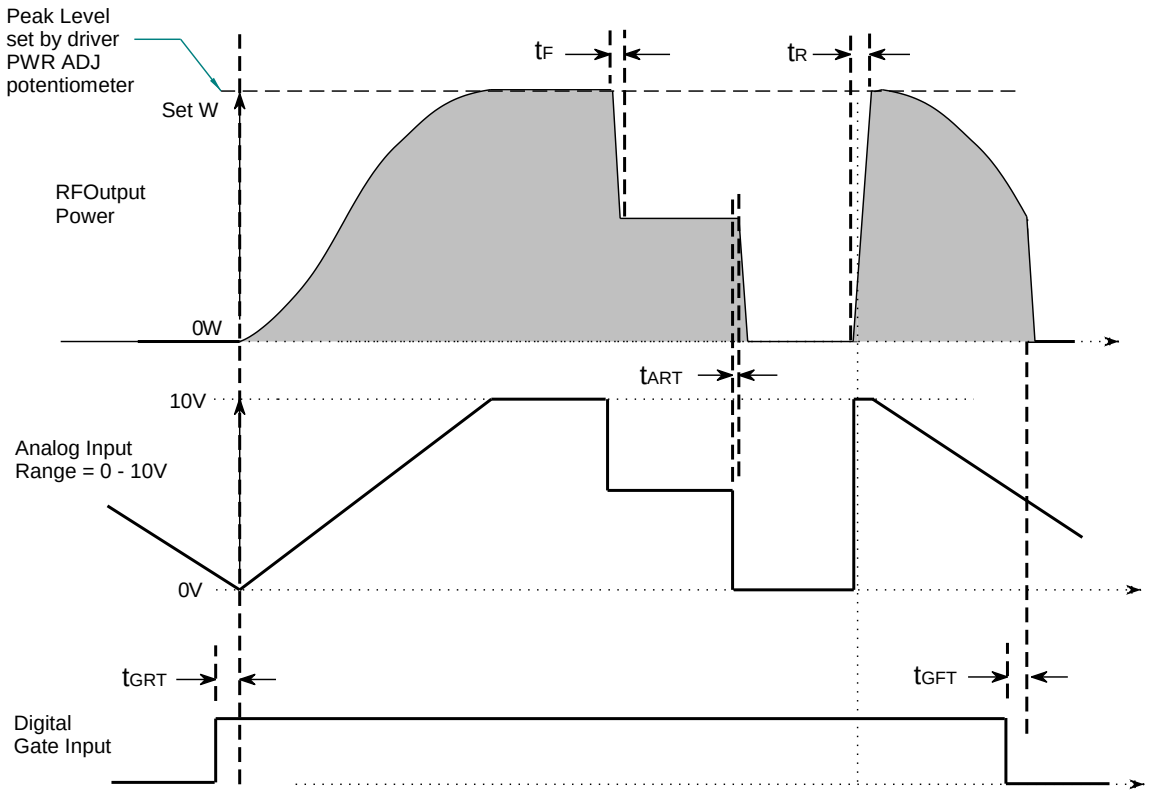



Figure 1: Typical Analog Modulation Waveforms

Timing Specifications




| Ident | Description | Max |
|---|---|---|
| $t_R$ | RF rise time resulting from 'large signal' analog modulation | 250 ns |
| $t_R$ | RF rise time resulting from TTL modulation (Option –DA) | 300 ns |
| $t_F$ | RF fall time resulting from 'large signal' analog or TTL: modulation | 100 ns |
| $t_{ART}$ | Delay between a change in Modulation input and the resultant change in RF output | 250 ns |
| $t_{GRT}$ | Delay between a change in digital Gate input and RF fully enabled | 0.5 ms |
| $t_{GFT}$ | Delay between a change in digital Gate input and RF fully disabled | 2.5 ms |

Signal description

**Gate (active high enables the RF amplifier)**

PLC compatible opto-isolated input

Default condition is RF Off.

A high level (5V < V < 24V) will gate the RF **ON**.

A low level (0V < V < 4V), or not connected will gate the RF **OFF.**

**Analog Modulation (0 - 10V)**

Provides high speed proportional amplitude control of the RF output.
Lower limit: an input voltage of less than 0.4V will drive the RF Off.
Upper limit: an input of 10V will result in the maximum RF output,

(For RFA651D type, this modulation control is simple On:Off and requires a 5V CMOS / TTL compatible input).

The amplitude level is defined by the selected RF power adjustment POT.

**RF Power Adjustment (POT set level)**

The maximum RF power limit is set by one of two methods. The method is selectable by the user.

a) A manual adjust multi-turn potentiometer 'PWR ADJ' for each frequency.
Maximum RF power = fully clockwise

or

b) A quad 256 step digital potentiometer configured to give independent power control with variable end limits

Three channels are used for power level control. RDAC0, RDAC1, and RDAC3
(see AD5254 data sheet). Levels are set remotely via an I2C compatible serial connection.
The slave address for the digital I2C potentiometer is at 0101100. (AD0 = AD1 = 0)

**DC Power**

A low impedance DC power supply is required. The operating voltage is +24Vdc only at a current drain of approximately < 14A. The external power source should be regulated to ± 2% and the power supply ripple voltage should be less than 200mV for best results. Higher RF output power is achieved at 28Vdc.

### 2.1 Thermal Interlocks

The AOM and Driver are fitted with thermostatic switches which will switch open circuit if a predetermined temperature is exceeded. These thermal interlocks will reset once the AO device and / or RF driver are cooled below this temperature.

- The driver thermal switch over-temperature threshold is 50deg C
- The AOM750 series thermal switch over-temperature threshold is 32deg C

The hysterisis of the thermal switches is 7-10deg C.
Once in a fault state the coolant temperature will need to be reduced to reset the thermal switches.

## Precautions

**Analog levels must not exceed 15 volts positive, or -0.5 volts negative**

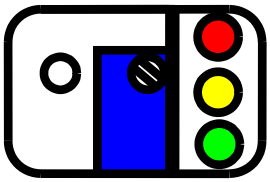
**PLC logic input levels must not exceed 24 volts**

**Water cooling is mandatory.**
**The heatsink temperature must not exceed 70°C.**
**Corrosion inhibitor should be added to the cooling water**

**SERIOUS DAMAGE TO THE AMPLIFIER MAY RESULT IF THE TEMPERATURE EXCEEDS 70°C. SERIOUS DAMAGE TO THE AMPLIFIER MAY ALSO RESULT IF THE RF OUTPUT CONNECTOR IS OPERATED OPEN-CIRCUITED OR SHORT-CIRCUITED.**

## 2.2 LED Indicator and Monitor outputs

The front panel tri-colour LED indicates the operating state.



(RF PWR ADJ) 50MHz LED

RED

The top LED will illuminate RED when there is a poor VSWR load (High reflected RF power fault).

**Normal condition is OFF**

A fault signal is triggered when the reflected RF power exceeds approximately 50% of the average forward power for more than 1 second. This fault is latching and the driver is disabled (RF power will go to zero). This fault can occur if the RF connection between the AOM and driver is broken.

Resetting

Once the fault condition is corrected, it will be necessary to reset the driver.

1) Turn the DC power OFF and ON

   or

2) Press momentary RESET button on driver located to right to the D-type

YELLOW

The middle LED will illuminate YELLOW, when the RF outputs are live and provided that

a) the Gate duty cycle is more than 20% (approx).

b) the RF average power is > 30W (approx)

**Normal condition is ON,** but may be OFF if the above conditions are not met

GREEN

The lower LED will illuminate GREEN when the following signals are all true:

1) RF DC power is applied and
2) Interlocks are valid and
3) GATE input is high.

**Normal condition is ON**

LEDS Off

The GREEN and/or YELLOW LED's will not illuminate if :

a) the internal driver thermal interlock switch is open (Over temperature fault)

b) the AOM thermal interlocks switch is open (Over temperature fault)

c) the AOM thermal interlock is not connected to the driver interlock input

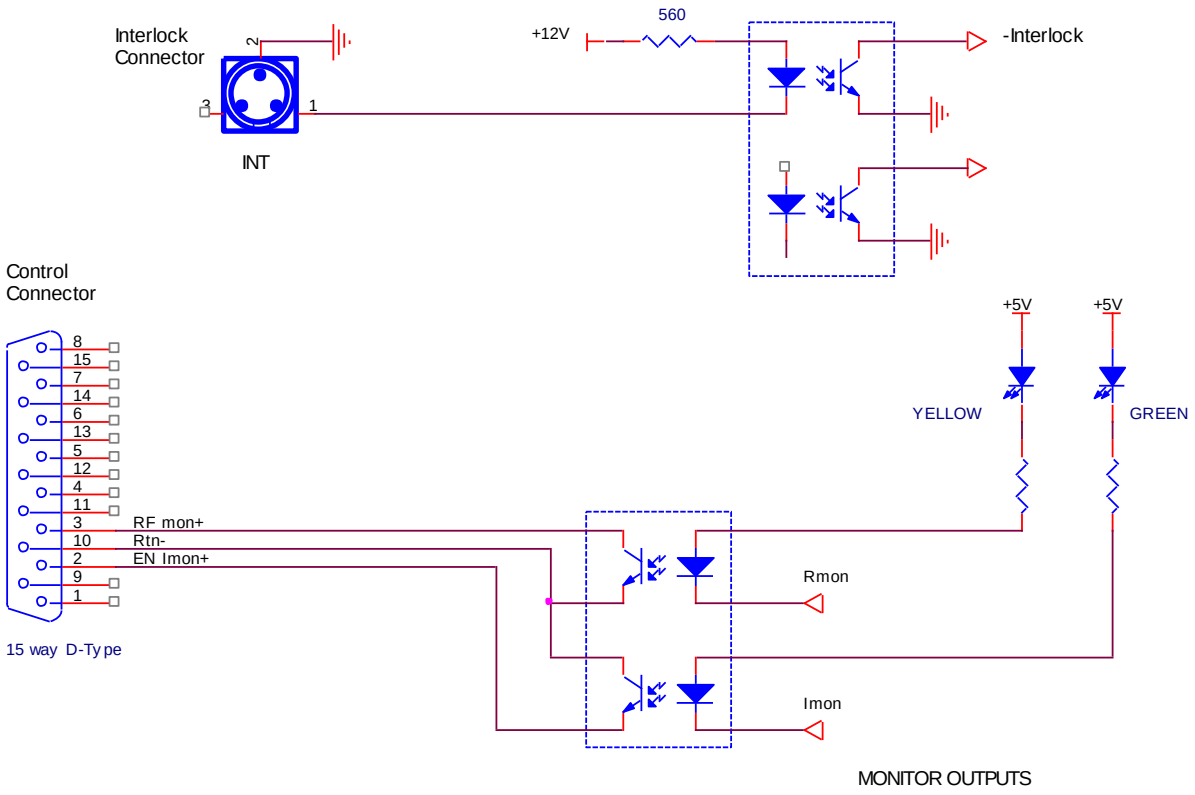
d) the DC supply is off.

The RED LED should be OFF

Monitor Outputs

The status of the YELLOW and GREEN LEDS is available at the D-type connector

These outputs are opto-isolated .




"Enabled" = low impedance between pins 2 and 10 = Green LED ON

"RF Active" = low impedance between pins 3 and 10 = Yellow LED ON

## 3. INSTALLATION AND ADJUSTMENT

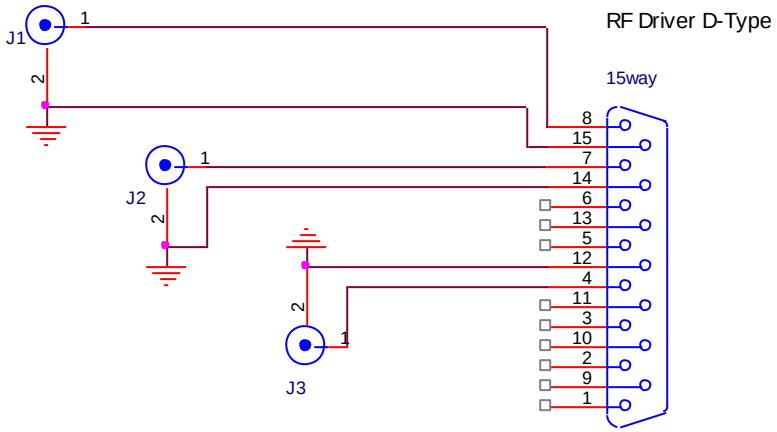
The basic set-up below is described using the manual RF power limit adjustment.

The remote power adjustment is described from 3.15 onwards. The driver will default to manual adjustment unless the remote power adjustment is selected (input S0)

J1 = Digital GATE / RF Enable input
PLC compatible
Logic HIGH (5V < V < 24V) = ON
Logic LOW (0V < V < 4V) = OFF

J2 = DIGITAL MODULATION input
TTL compatible levels
Logic HIGH (2.7V < V < 5V) = On
Logic LOW (0V < V < 0.8V) = Off

J3 = ANALOG MODULATION input
0V (off) - 10V( max on)




3.1 Connect cooling water to the RFA651

Connect cooling water to the AO device.

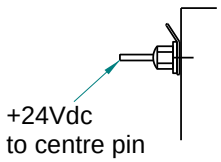
Refer to Figure 2. Use of a Corrosion inhibitor is strongly advised.

Due to the high RF power dissipated in the AO modulator, it is paramount that the device is operated only when water cooling is circulating.

For optimum AO performance ensure the flow rate is more than 2 litres/minute at < 20 deg.C

3.2 With no d-c power applied, connect the + 24V (or +28V) DC in to the center terminal of the feed-thru terminal. Connect 0V to ground tab or screw terminal. (See page 15).

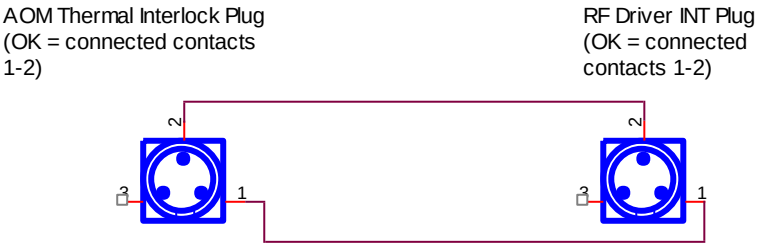
DO NOT turn on DC supply until step 3.8.




3.3 Connect the TNC output RF connector to the acousto-optic modulator TNC RF input (or a 50Ω RF load, if it is desired to measure the RF output power).

3.4 Connect the Interlock of the acousto-optic modulator (mini 3-pin snap connector) to the RF driver “INT” input (mini 3-pin snap connector). Connect pin 1 to pin 1 and pin 2 to pin 2.

If the temperature of the modulator exceeds 32ºC or the internal driver temperature exceeds 50ºC then the interlock connection becomes open circuit, disabling the RF output. An LED indicator illuminates when the Interlocks are closed and the RF is enabled. In addition, a open drain ‘interlock valid’ signal output is provided on pin 2 of the D-type connector for remote monitoring purposes.




3.5 Adjustment of the RF output power is best done with amplifier connected to the acousto-optic modulator. When shipped, the Amplifier maximum output power is set to approx 100W selecting the manual PWR ADJ pot and 120W for the digital pots.

The optimum RF power level required for the modulator to produce maximum first order intensity will be differ depending in the laser wavelength. Applying RF power in excess of this optimum level will cause a decrease in first order intensity (a false indication of insufficient RF power ) and makes accurate Bragg alignment difficult. It is therefore recommended that initial alignment be performed at a low RF power level.

3.6 Locate the PWR ADJ on the driver end plate.
The 50MHz RF Power adjuster is adjacent to the LED stack

3.7 With an insulated alignment tool or screwdriver rotate the PWR ADJ potentiometer fully anti-clockwise (CCW) i.e. OFF, then clockwise (CW) approx 5 turns.

3.8 Ensure cooling water is connected and flowing. Apply DC to the amplifier.

3.9 Apply a 10.0V constant modulation signal to the modulation
Connect pin 4 of 'D' to the signal and pin 12 of 'D' to the signal return (0V).
(For RFA651-D, apply a constant TTL=H to pin 4)
(For RFA651-DA, also apply a constant TTL=H to **pin 7**)

3.10 Apply a constant PLC **high** level (typically 12V or 24V) to the digital gate input on the D-type connector. Connect pin 8 of the 'D' to the Signal and pin 15 of the 'D' to the signal return.

3.11 If using the remote power adjust, apply a constant PLC **low** level (less than 2V) to the POT SELECT input (S0) on the D-type.
Connect pin 1 of the 'D' to the Signal and pin 9 of the 'D' to the signal return.
A low level (or no connect) will enable power adjustment using the Manual pots.

If using the Manual adjust PWR POT only, then make no connection to pin 1

Input the laser beam toward the centre of either aperture of the AOM. Ensure the polarization is horizontal with respect to the base and the beam height does not exceed the active aperture height of the AOM. Start with the laser beam normal to the input optical face of the AOM and very slowly rotate the AOM (either direction). See Figure 4 for one possible configuration.

3.12 Observe the diffracted first-order output from the acousto-optic modulator and the undeflected zeroth order beam. Adjust the Bragg angle (rotate the modulator) to maximise first order beam intensity with the 50MHz Frequency selected.

3.13 After Bragg angle has been optimized, slowly increase the RF power by turning PWR ADJ clockwise until maximum first order intensity is obtained.

**The optimum RF power level required for the modulator to produce maximum first order intensity will be different at various laser wavelengths. Applying RF power in excess of this optimum level will cause a decrease in first order intensity (a false indication of insufficient RF power ) and makes accurate Bragg alignment difficult. It is therefore recommended that initial alignment be performed at a low RF power level.**

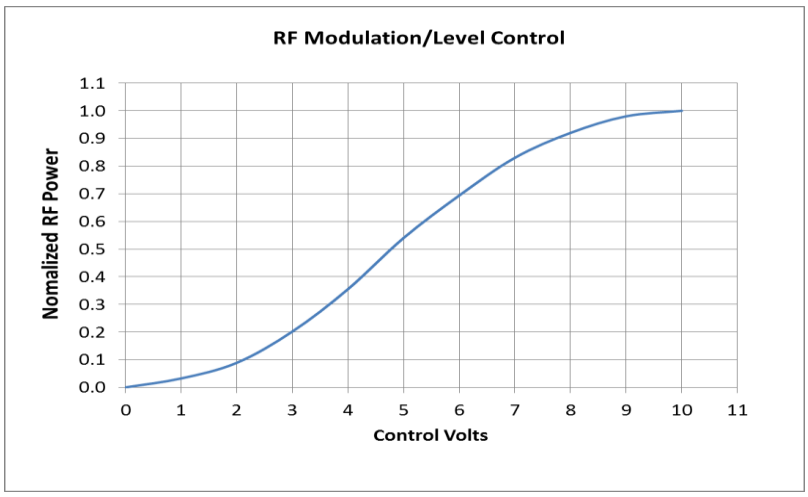
### *3.14 Analog Modulation / Manual RF Power Level Control*

The analog modulation input can also be used for remote analog power control of the driver.
e.g. Set the Manual PWR ADJ POT to maximum* and use the analog input to control the driver output power from zero to maximum power.
*For best dynamic range, the Manual PWR ADJ POT should be set so that the RF driver power is limited to the AOM *Psat* value at the maximum Analog modulation input (see below)

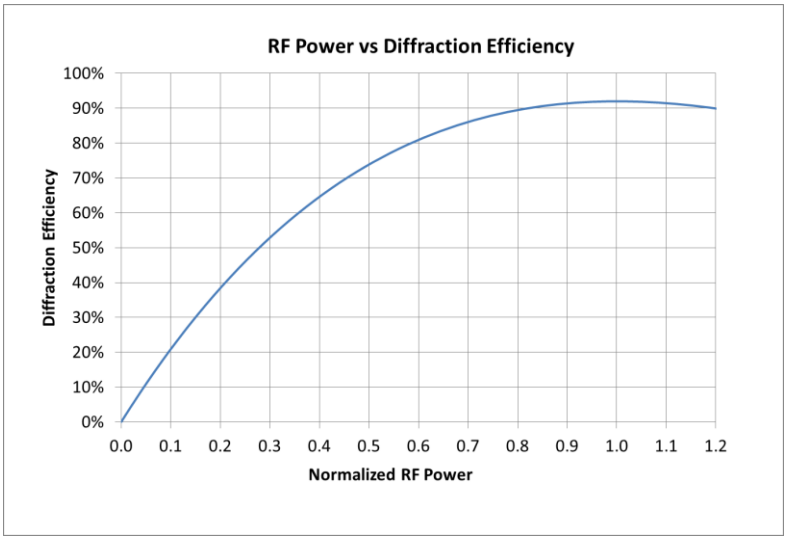
### 3.15 RF Power and Psat

Plots below show the typical generic responses RF powers are normalized to Psat.
*Psat = Optimum RF power level for maximum 1$^{st}$ order diffraction efficiency.*
The AO test data sheet will give the Psat value for that model.
Applying RF power in excess of Psat will lead to a reduction in efficiency and increased thermal load.

Typical RF output Power vs. Analog Modulation Input (0-10V)




Typical First Order Diffraction Efficiency vs. RF Input Power

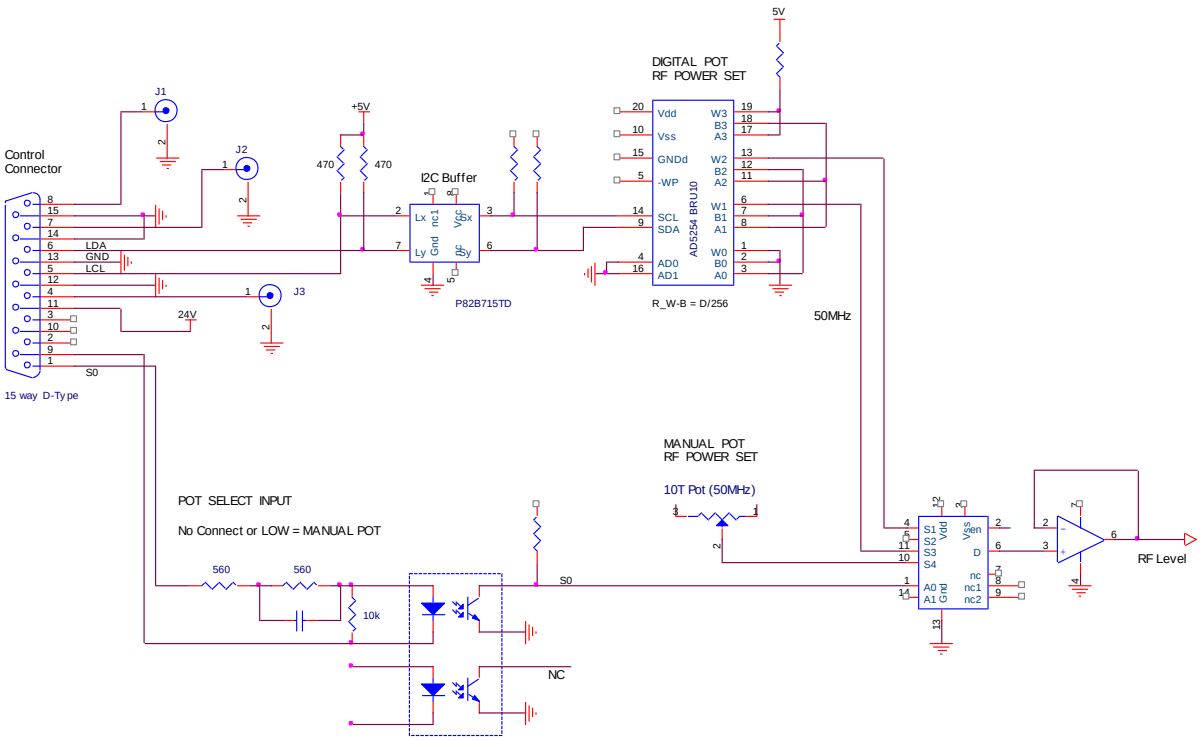


### *3.16 Remote Digital RF Power Adjust*

To enable remote RF power control using the digital POT, connect pin1 (S0) of the 15way D-type control driver connector to a PLC compatible logic port . Apply a high signal.

The RF power may be adjusted remotely using an I2C compatible interface. The control circuit is based on the Analog Devices non-volatile 256 step digital potentiometer AD5254. The Analog Devices on-line data sheet describes the communication protocol.

The slave address for the digital I2C potentiometer is at 0101100. (AD0 = AD1 = 0)
Maximum resistance equates to maximum RF power.
The digital potentiometer value is non-volatile and will recall the last saved value on power-up.



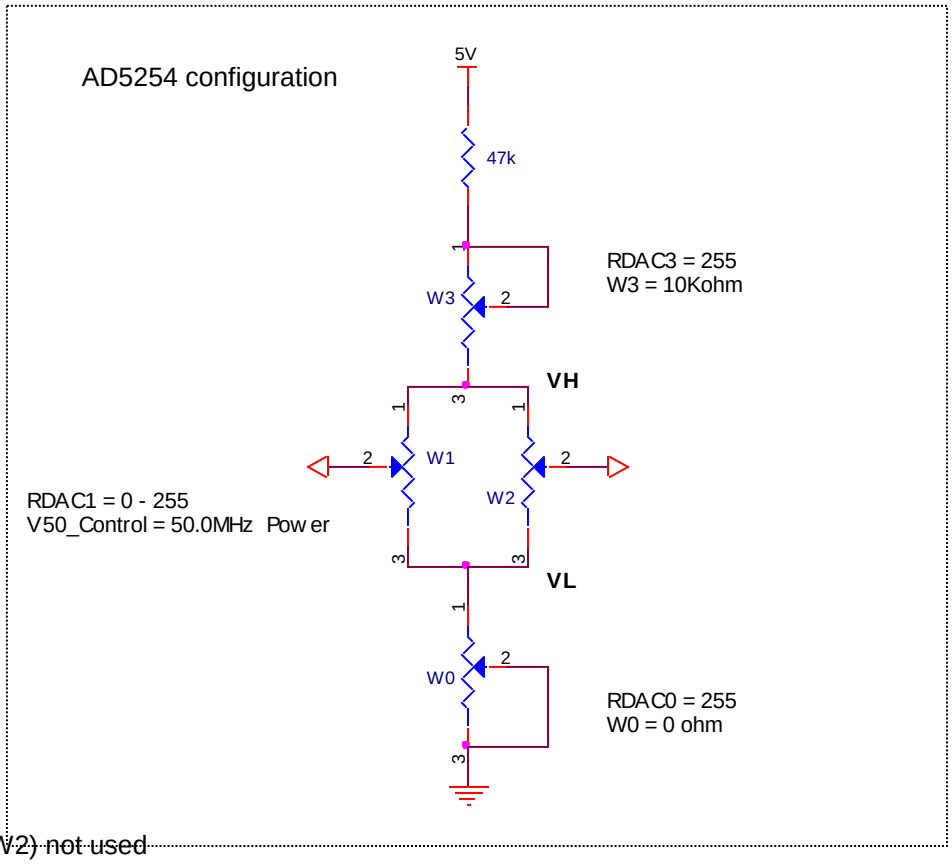

The modulation control inputs J1,J2 and J3 are not shown for clarity

DO NOT exceed +5V on the I2C Inputs, LDA (data IO) and LCL (clock)
The I2C signals are buffered using the bus extender chip P82B715 from NXP

The four digital pots are configured into a potential divider.

The main power control pot W1 is in parallel with W2 and thus equates to 5Kohm resistance.

The upper and lower limit adjustment Pots W3 and W0 apply to both W1 and W2.




RDAC2 (W2) not used

RDAC1 defines the 50 MHz power control factor

V50_Control = VL + (VH-VL) x W1/255

where W1= 8-bit value programmed into RDAC1

RDAC0 defines the lower limit pot

Lower pot resistance R_W0 = (255-W0)/255 x 10Kohm

Lower limit voltage VL = (R_W0) / (47K+R_W3+5K+R_W0)

RDAC3 defines the upper limit pot

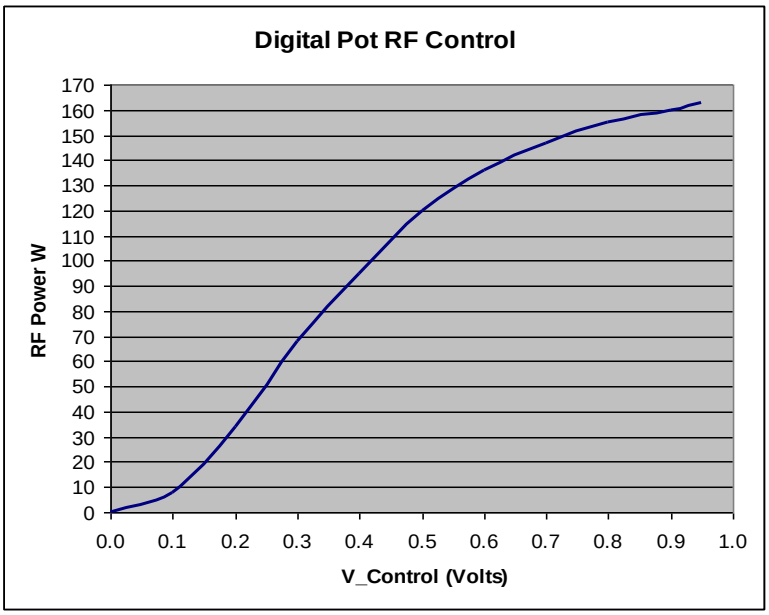
Upper pot resistance R_W3 = (W3)/255 x 10Kohm

Upper limit voltage VH = (R_W0+5K) / (47K+R_W3+5K+R_W0)

The full range power adjustment is shown below.

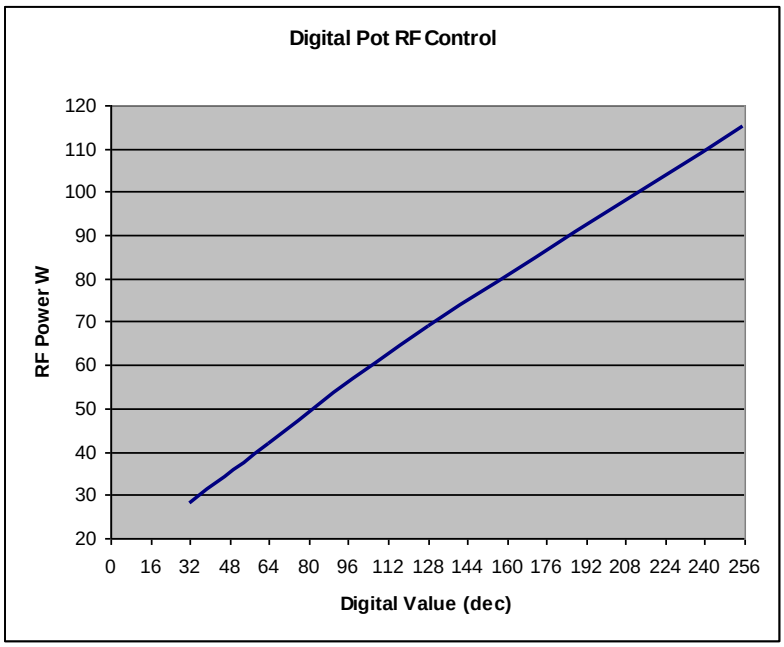
Settings: RDAC3 = 0 (R_W3=0k) and RDAC0 = 255 (R_W0=0k).

The V_Control scale equates to 0 – 255 adjustment range on RDAC1 (W1)




By adjusting the values of RDAC0 and RDAC3 it is possible to increase the adjustment resolution of the 8-bit power level control at 50.0 MHz (RDAC1) over a defined range.

A typical Digital Power curve is shown below. In this case settings are: RDAC3 = 255 (R_W3=10k) and RDAC0 =t 200 (R_W0=2K)



## 4. MAINTENANCE

### 4.1 Cleaning

It is of utmost importance that the optical apertures of the deflector optical head be kept clean and free of contamination. When the device is not in use, the apertures may be protected by a covering of masking tape. When in use, frequently clean the apertures with a pressurized jet of filtered, dry air.

It will probably be necessary in time to wipe the coated window surfaces of atmospherically deposited films. Although the coatings are hard and durable, care must be taken to avoid gouging of the surface and leaving residues. It is suggested that the coatings be wiped with a soft ball of brushed (short fibres removed) cotton, slightly moistened with clean alcohol. Before the alcohol has had time to dry on the surface, wipe again with dry cotton in a smooth, continuous stroke. Examine the surface for residue and, if necessary, repeat the cleaning.

### 4.2 Troubleshooting

No troubleshooting procedures are proposed other than a check of alignment and operating procedure. If difficulties arise, take note of the symptoms and contact the manufacturer.

### 4.3 Repairs

In the event of deflector malfunction, discontinue operation and immediately contact the manufacturer or his representative. Due to the high sensitive of tuning procedures and the possible damage which may result, no user repairs are allowed. Evidence that an attempt has been made to open the optical head will void the manufacturer's warranty.

RFA651 **Connection Summary**

1.0 15 way 'D' Type Control Connection

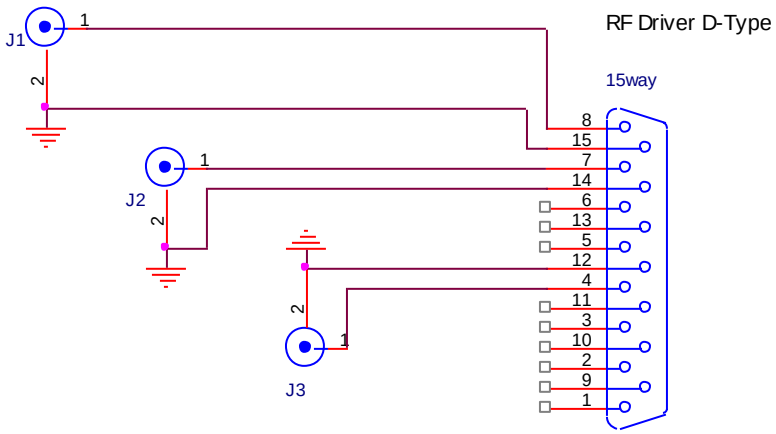
| Signal (see notes) | Type | Pin out connection |
|---|---|---|
| NECESSARY | | |
| (All driver options)<br>Digital Gate **<br>PLC high (5v<V<24v) = ON<br>PLC low (0.0v<V<4v) or NC = OFF | Input | Signal pin 8<br>Return pin 15 |
| *RFA651 or RFA651-DA*<br>Analogue Modulation *<br>< 0.4V(off) to 10.0V(on) | Input | Signal pin 4<br>Return pin 12 |
| - or - | | |
| *Option -D*<br>*RFA651-**D***<br>Digital Modulation *<br>TTL high (2.7v<V<5.0v) = ON<br>TTL low (0.0v<V<0.8v) = OFF | Input | Signal pin 4<br>Return pin 12 |
| - and - | | |
| *Option –DA only*<br>*RFA651-**DA***<br>Digital Modulation *<br>TTL high (2.7v<V<5.0v) = ON<br>TTL low (0.0v<V<0.8v) = OFF | Input | Signal pin 7<br>Return pin 14 |
| Interlock ***<br>Normally closed | Input | Connect to AOM "INT" |
| OPTIONAL | | |
| 'Enabled' monitor<br>(Open collector logic, Low = OK)<br>**Maximum applied voltage (via external pull up resistor) = 24V**<br>Maximum current = 20mA | Output | Signal pin 2<br>Return pin 10 |
| 'RF Status' monitor<br>(Open collector logic, Low = OK)<br>**Maximum applied voltage (via external pull up resistor) = 24V**<br>Maximum current = 20mA | Output | Signal pin 3<br>Return pin 10 |
| I2C Clock<br>(0.0v<V<5.0v) | Input | Signal pin 5<br>Return pin 13 |
| I2C Data IO<br>(0.0v<V<5.0v) | In/Out | Signal pin 6<br>Return pin 13 |
| POT Select Control, S0<br>PLC high (5v<V<24v) = Digital Pot<br>PLC low (0.0v<V<4v) or NC = Manual Adjust | Input | Signal pin 1<br>Return pin 9 |

## RFA651-DA Modulation (dual) and Gate Input connections

J1 = Digital GATE / RF Enable input
PLC compatible
Logic HIGH (5V < V < 24V) = ON
Logic LOW (0V < V < 4V) = OFF

J2 = DIGITAL MODULATION input
TTL compatible levels
Logic HIGH (2.7V < V < 5V) = On
Logic LOW (0V < V < 0.8V) = Off

J3 = ANALOG MODULATION input
0V (off) - 10V( max on)

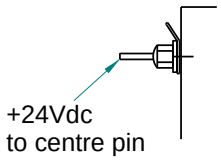



## Interlock connection

AOM Thermal Interlock Plug
(OK = connected contacts 1-2)

RF Driver INT Plug
(OK = connected contacts 1-2)

## DC supply connection for drivers fitted with solder feed through




Case stud = 0V

**Notes:**

*** The interlock signal must be connected. Contacts closed for normal operation.

2.0 Mounting Holes: 4 off M5

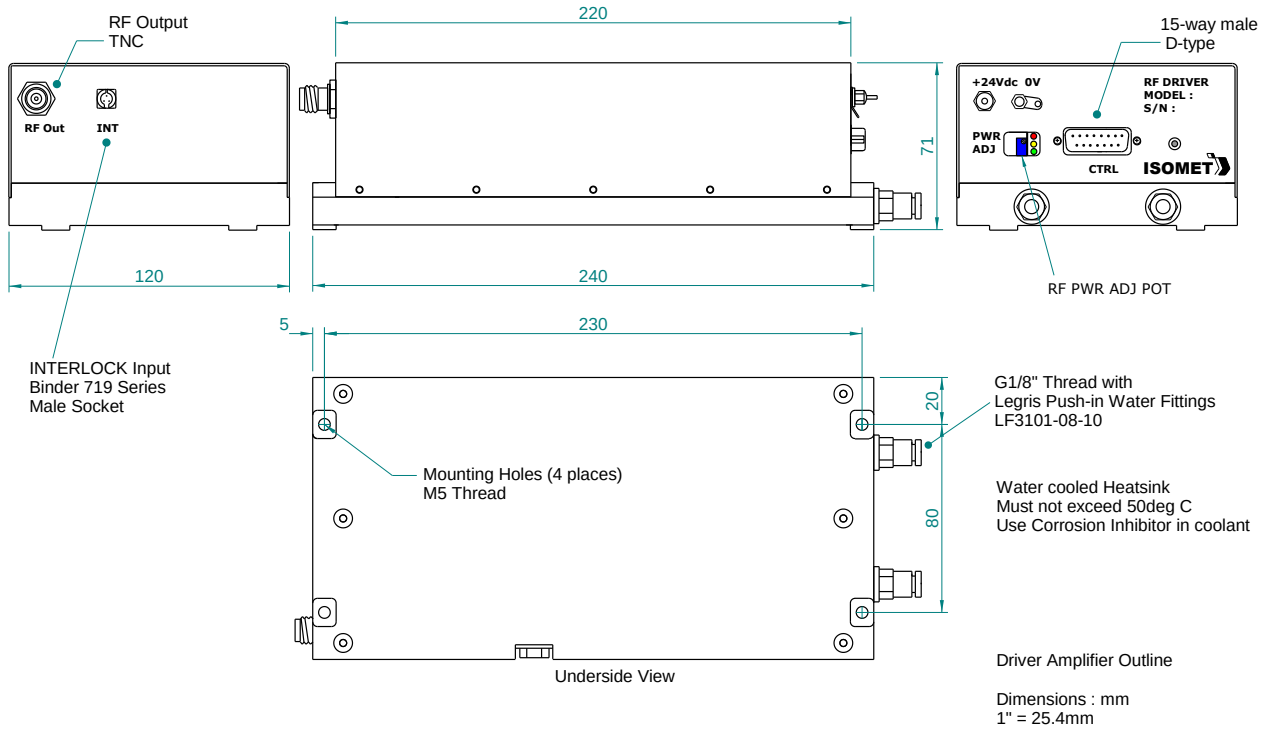



Figure 2: Driver Installation

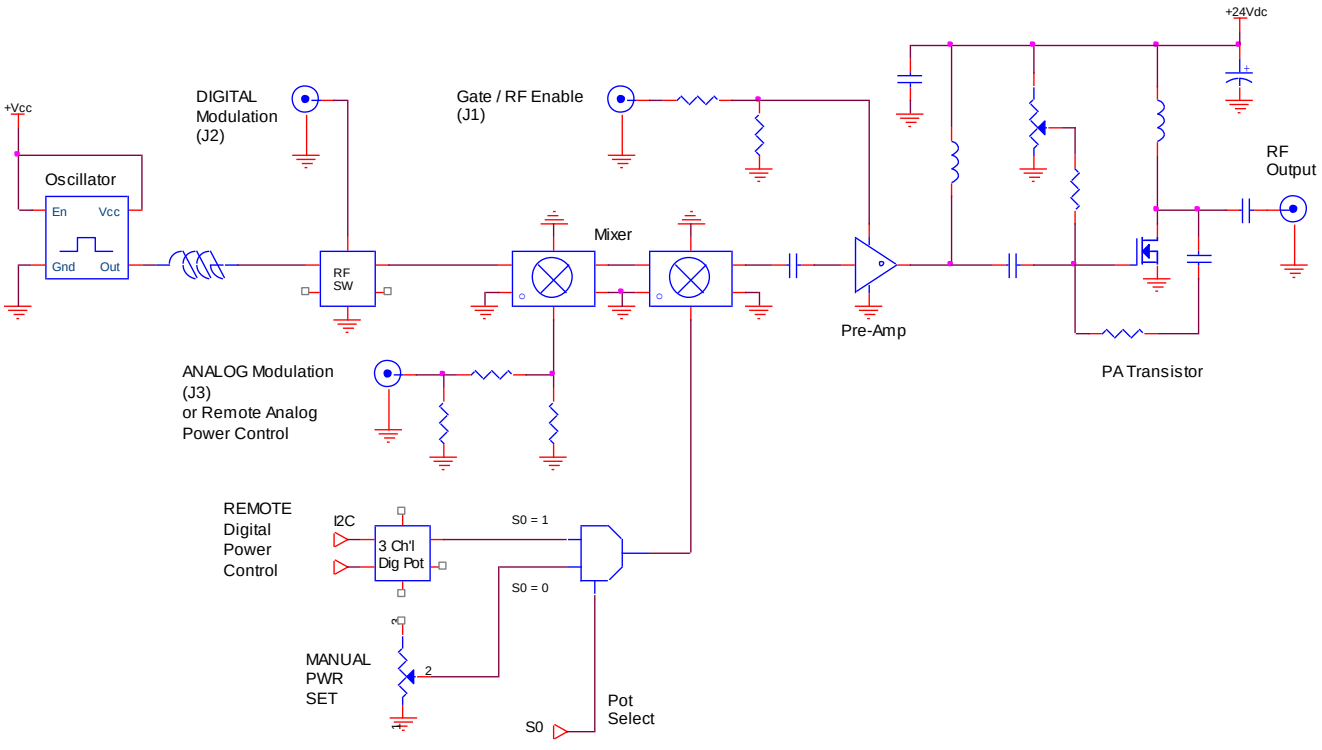



Figure 3: Driver Block Diagram

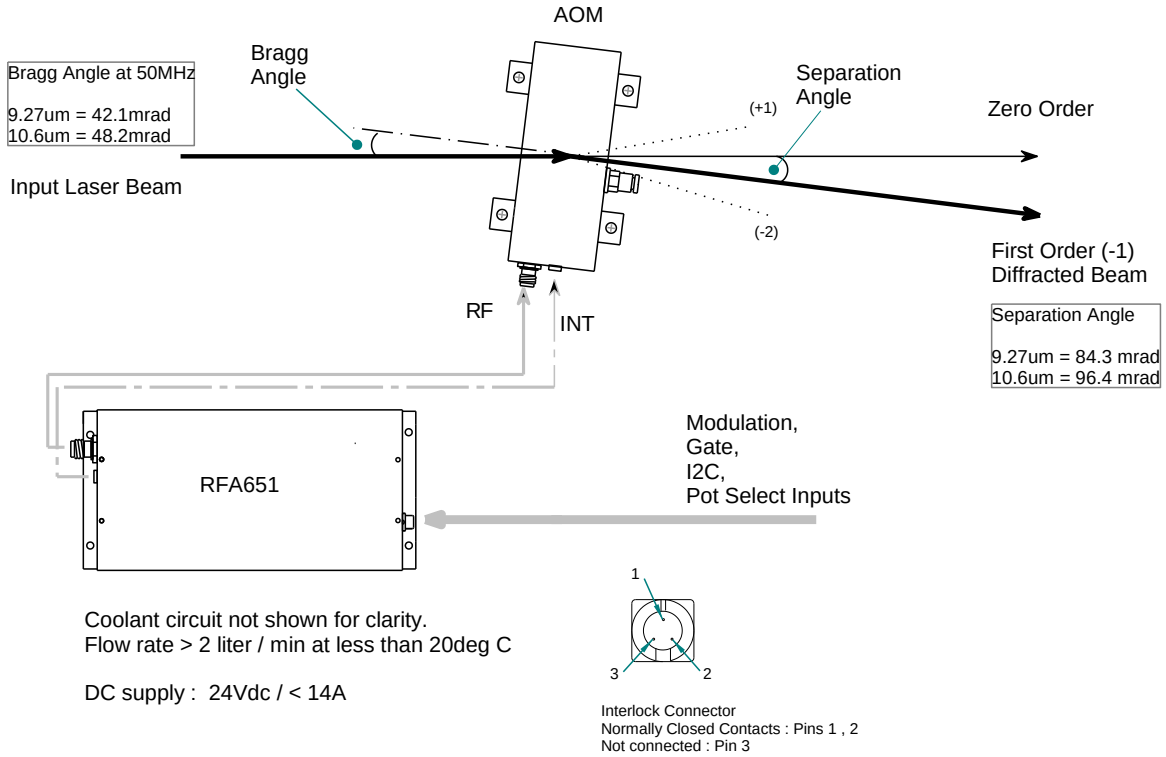



Figure 4: Typical Connection Configuration using RFA651 series.

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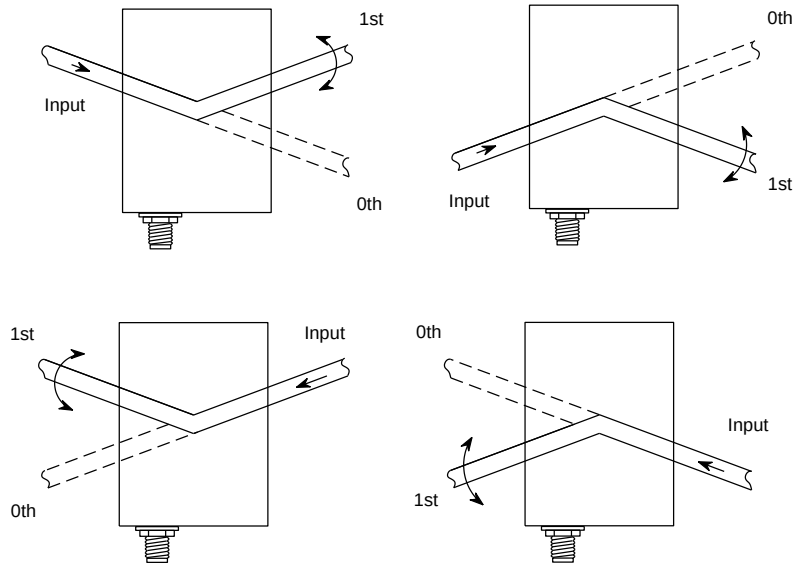
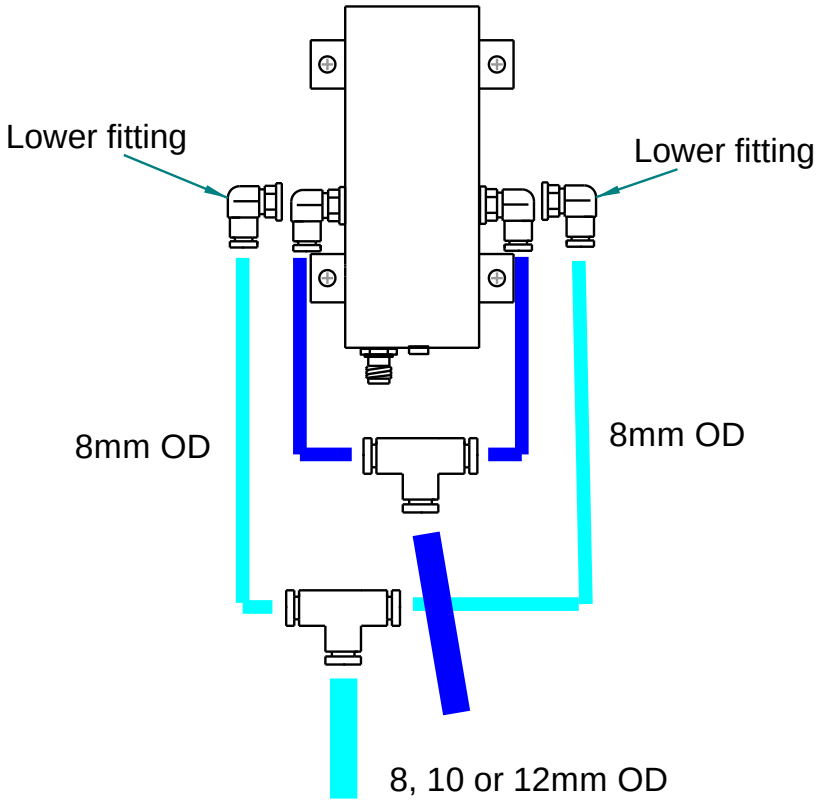
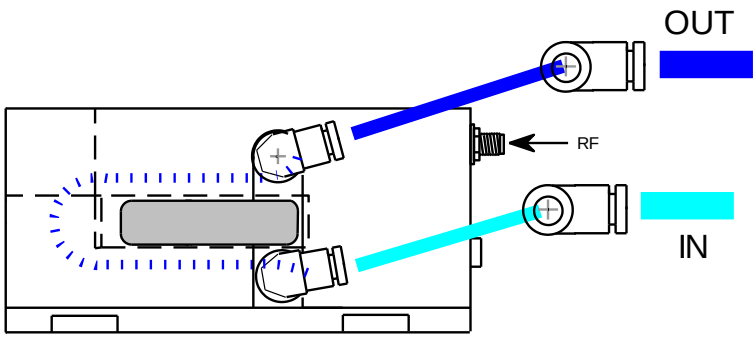
**Orientation options**



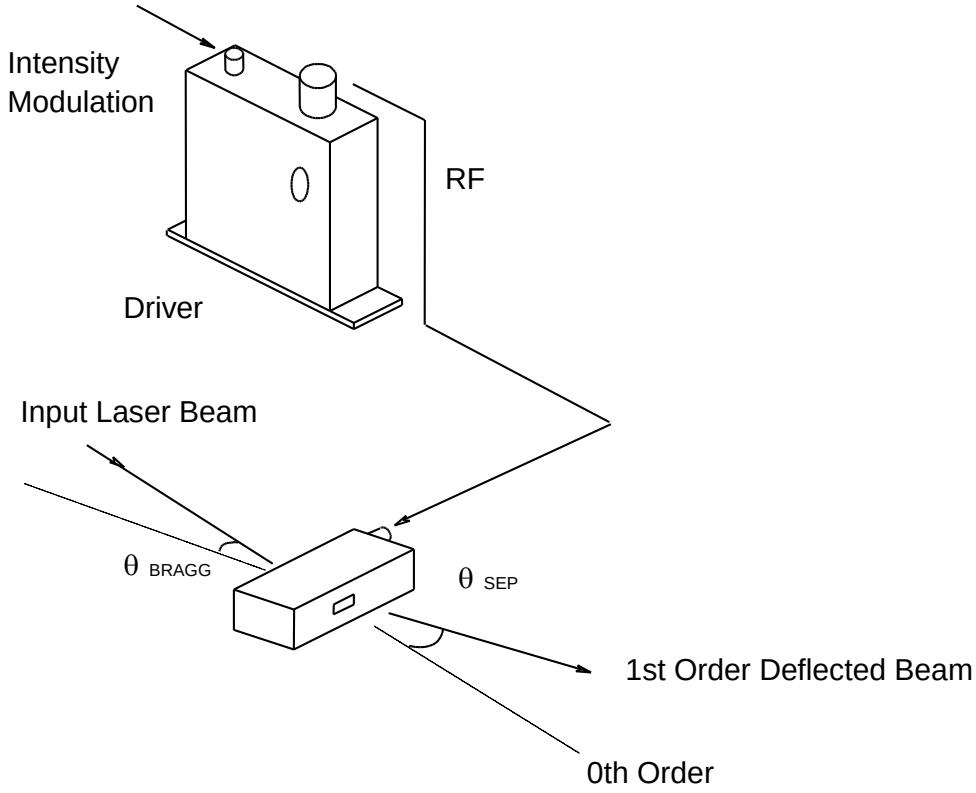
**AOM700 / M1199 / M1192 coolant flow**

Flow rate enhancement using dual fittings and T-piece



**Basic AO Modulator Parameters**




The input Bragg angle, relative to a normal to the optical surface and in the plane of deflection is:

$$\theta_{BRAGG} = \frac{\lambda.fc}{2.v}$$

The separation angle between the Zeroth order and the First order is:

$$\theta_{SEP} = \frac{\lambda.fc}{v}$$

Optical rise time for a Gaussian input beam is approximately:

$$t_r = \frac{0.65.d}{v}$$

where: $\lambda$ = wavelength
fc = centre frequency = 50MHz (see AOM data sheet)

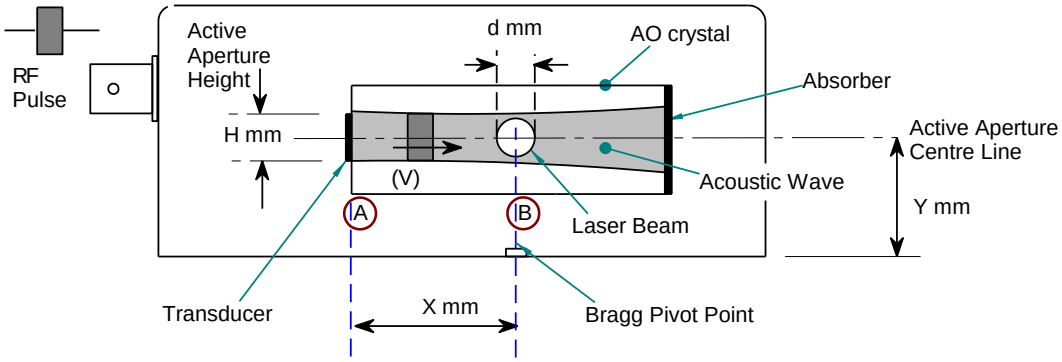
v = acoustic velocity of interaction material = 5.5mm/usec (Ge)
d = $1/e^2$ beam diameter

Figure 5. Modulation System

## Appendix A: Beam Position

Timing and delay considerations

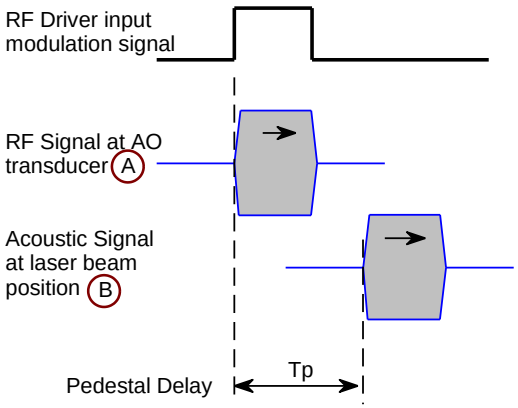
When attempting to synchronize a pulsed laser beam with a pulsed RF acoustic wave in an AO device, the designer must consider the transit time of the acoustic wave from the transducer to the laser beam position. This is called the Pedestal delay.



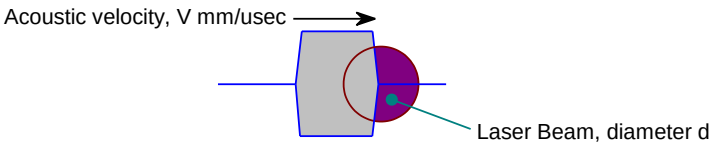

Input Beam Location
Vertical axis: Place the laser beam at the centre of the active aperture at Ymm above the base.
Horizontal (Diffraction) axis : Place beam above the Bragg pivot point.

Timing considerations with respect to the RF modulation signal:
Acousto-optics are travelling wave devices. The acoustic wave is launched from the transducer and travels at velocity V across the laser beam and into the absorber.

1: Pedestal delay = time for the acoustic wavefront to reach the laser beam.
Tp = beam position from transducer (X) / acoustic velocity (V)




2: Transit time = time for the acoustic wavefront to cross the laser beam.
Tt = beam diameter (d) / acoustic velocity (V)
Optical switching time for a Gaussian beam is approximately 0.65 x Tt



Example:

For the AOM650, AOM750, M1199 series of $CO_2$ Germanium AO modulators/deflectors, the Bragg pivot point is located at X = 30mm from the transducer (+/- 1mm)

(Note: the M1199 may have a 2nd pivot hole, 22mm from the transducer)

The Acoustic velocity in Germanium is 5.5 mm/usec.

Thus, for a laser beam placed above the Bragg Pivot point

Pedestal delay = 30/5.5 = 5.46 usec

The pedestal delay will depend on the AO model and the actual laser beam position.

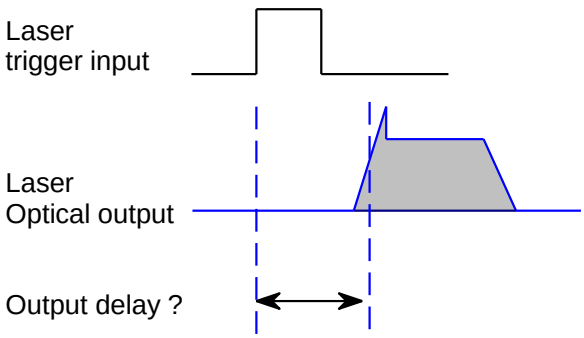
For an 8mm input beam diameter,

Transit time = 1.46 usec

(Note: The optical rise time for a Gaussian beam is approximated by 0.65 x transit time)

<u>Laser synchronization</u>

Please be aware, depending on the Laser type, there may be a significant delay between the laser input trigger signal and the actual laser optical output pulse.




This should be considered when synchronizing the laser and pulsed RF (acoustic) waves.